Simultaneous Chip-Join and Underfill Assembly Technology for Flip-Chip Packaging

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Index words: C4, underfill, packaging, flip chip

ABSTRACT

Controlled Collapse Chip Connection (C4) flip-chip packaging is the current state of the art assembly technique. The C4 Organic Land Grid Array (OLGA) technology process to attach a silicon die to a package substrate involves seven process steps.

In the current plan of record (POR) C4 OLGA flip-chip assembly process, solder wetability is achieved by removing Pb/Sn oxide films from the bump material by means of a flux and deflux process. An epoxy material is placed between the die and package. This underfill (UF) process has a long epoxy application step and curing time.

We present a three-step chip-join assembly process using a no-flow-type underfill material combined with non-lead-containing bump metal on the chip side. This process has fewer process steps than the POR assembly process, and the underfill cure time is also reduced.

The process described in this paper shortens the assembly process by eliminating fluxing, defluxing, and furnace reflow steps. We achieved more than a 90% assembly yield as a result of process parameter and material property optimization.

INTRODUCTION

Intel successfully introduced C4 OLGA technology into the Personal Computer (PC) market in April 1998. The technology has many advantages over wire bonding and Tape Automated Bonding (TAB): it has a higher Input/Output (I/O) number, shorter interconnects, and the silicon die self-aligns to the package.

The current C4 OLGA plan of record (POR) process to attach a silicon die to a package substrate and apply the underfill material requires seven processing steps. An epoxy-type material is required in C4 packaging to prevent solder bumps on the silicon die from moving and electrically shorting during the life of the part. The underfill also mediates the thermal miss-match between the silicon die and the organic polymer package. The underfill material is applied in a liquid form to flow between the silicon C4 bumps and the package substrate. A high-temperature oven cure is required to set the polymer.

Several different underfill formulations and bump metals were examined. We found a correlation between the size of particles in the underfill material and silicon bump to package substrate joint reliability. Different underfill resins were tested. Resins causing a higher viscosity showed better reliability after a temperature cycle reliability test.

We examined the potential package assembly cost savings using our three-step process. By eliminating process steps and shortening the cure time, a substantial cost savings can be realized.

This paper describes an assembly technology that targets future-generation C4 flip-chip packaging. We report a method to combine silicon chip join and epoxy underfill processes in one step with a shorter underfill cure time. The process has fewer steps than the POR assembly process. The POR assembly is shown in Figure 1 with our new assembly process flow shown in Figure 2.

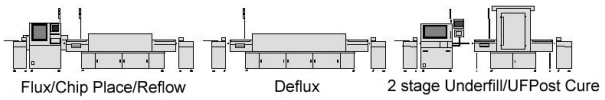

Figure 1: Current (P856) chip join assembly process

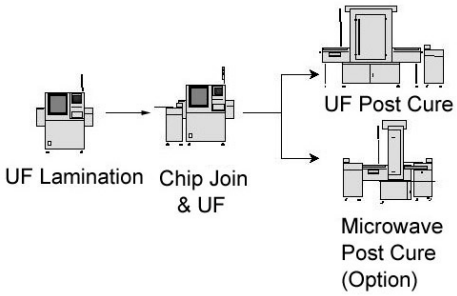

Figure 2: New one-step chip join assembly process

MATERIALS AND PROCESS

Materials

Die

Test die were used with different bump metal material. To obtain good adhesion between the bump material and die, a Ti/Au under bump metallurgy was used.

Substrate

The test substrate was an OLGA material with Sn/3.5Ag eutectic pre-solder paste.

UF Material

The no-flow-type underfill material provided by Nitto Denko was used in the testing. The UF properties of the first formulation are listed in Table 1[1].

Table 1: No-flow-type UF property

thickness	80μm
resin	non-conductive
CTE (below Tg)	41ppm/K
CTE (above Tg)	113ppm/K
gel time at 175 °C	23 seconds
Tg	117 °C
film size	12 x 12mm

Process

The new process has three steps: 1) UF lamination; 2) chip placement and UF cure, and solder reflow with a flip-chip bonder; and 3) post cure of UF. Figure 3 shows the chip-join assembly step. First, UF was manually laminated onto the substrate with a roller on a hot plate heated at 90°C. Second, chip join was performed with a semi-automatic bonding machine. The heat stage was set at 135°C. After chip placement, the temperature was ramped up to 192°C by the use of a head tool to cure the UF for 60 seconds. The temperature was increased to 230°C for solder reflow. Post-cure cool down was conducted at 150°C/1hr using a conventional oven.

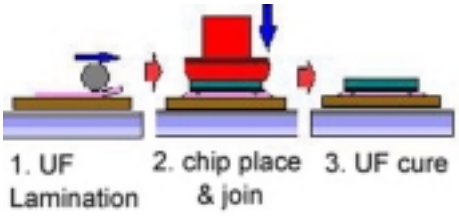

Figure 3: One step chip-join assembly process

Microwave Oven Reflow and Cure Process

To further reduce process time, we used a microwave oven to cure the UF epoxy. This replaced the conventional oven and flip-chip bonder reflow process. Using a microwave to cure the epoxy took less time than a conventional oven and a flip-chip bonder reflow process as shown in Figure 4. Therefore, assembly time will be reduced from 62 to 8 minutes per unit when the microwave cure is used in this new chip-join assembly process.

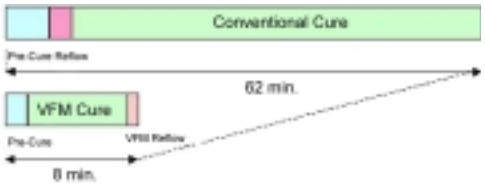

Figure 4: Microwave reflow and cure process for one-step chip-join assembly process

All samples using the microwave cure process passed the initial electrical test at the interconnection side of the solder joint. The sample size was 955 pieces in five substrate lots. However, we found that 9.2% of the failures on the substrate side of the solder joint were caused by an electrical open due to substrate cracking. Additional process characterization is required for microwave epoxy curing.

RESULTS

During development of this new assembly process, we found a joint problem after assembly. Assembly yield loss was due to an electrical open found in the peripheral area of the die.

Solder Flow-Out

Figure 5 and Figure 6 show the cause of the electrical open: solder flow-out from the interconnection.

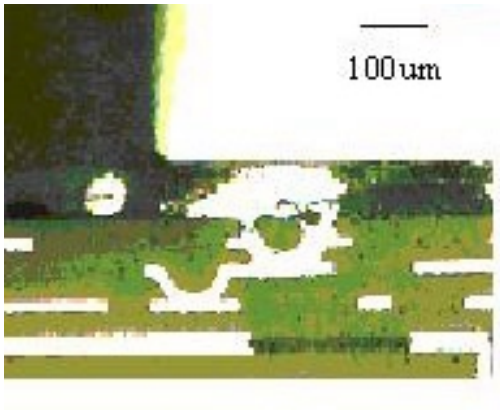

Figure 5: Solder flow-out from interconnection

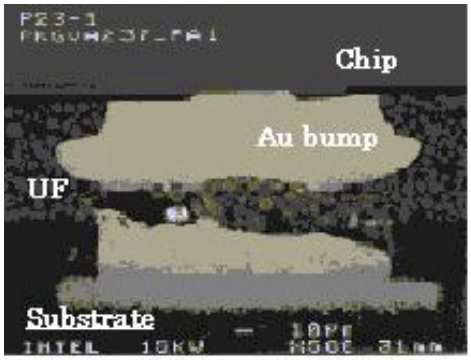

Figure 6: Solder flow-out from interconnection

Root Cause Analysis of Solder Flow-Out

Figure 7 shows the X-ray image of the solder flow-out from the interconnection before and after reflow. From the photo, it was found that solder flow-out happened during reflow. As a first step to eliminate this defect, the bonding force during reflow was reduced from 30kgf to 2kgf. An X-ray showed that solder flow-out was reduced by reducing the bonding, but not significantly.

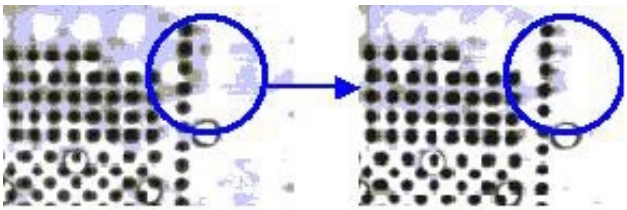

Figure 7: Solder flow after reflow

To determine the root cause of solder flow-out, the condition around bumps before reflow was examined. Figure 8 shows an X-ray image of the solder bumps on the silicon die.

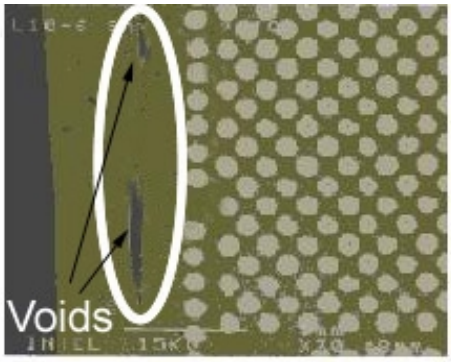

Figure 8: Underfill voids before reflow

The root cause of solder flow-out was void generation at the side of the bumps during die placement/cure, which was most likely caused by moisture absorption in the substrate. An experiment was conducted to compare the effect of substrate prebake against solder flow-out. Figures 9 and 10 show the X-ray views of the silicon bumps with and without substrate prebake. A significant reduction in voids was achieved with substrate bakeout; however, the voids were not completely eliminated.

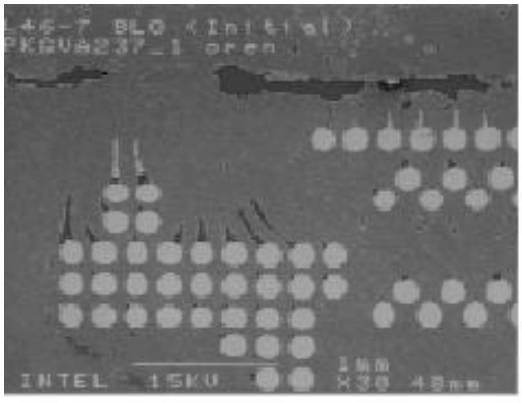

Figure 9: X-ray image of initial sample without prebake showing voids (dark areas) in the underfill material

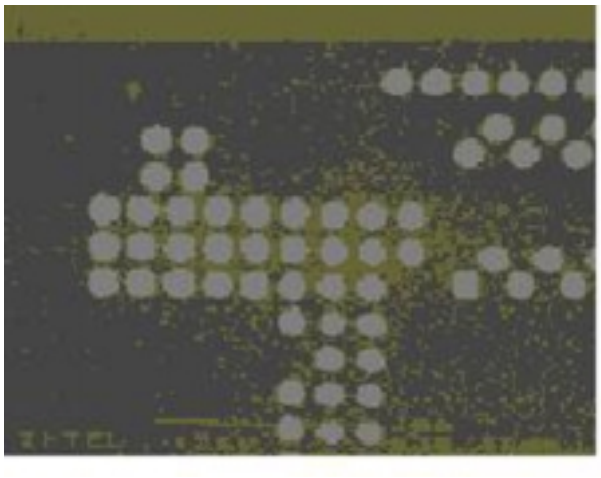

Figure 10: X-ray image of initial sample with prebake showing solder bumps

Rev 1 Baseline Assembly

We collected data for a Rev 1 baseline. Table 2 shows process conditions.

Table 2: Rev 1 baseline assembly process profile

Process Step	Condition
UF lamination	90 °C
UF cure/chip join	135 °C ramped to 192 °C for pre-cure, ramped to 228 °C for chip join
UF post cure	150 °C
total time	60 minutes

DISCUSSION

The assembly result showed 13/3000 pieces failed at the initial testing before reliability testing. Figure 11 lists the cause of each failure.

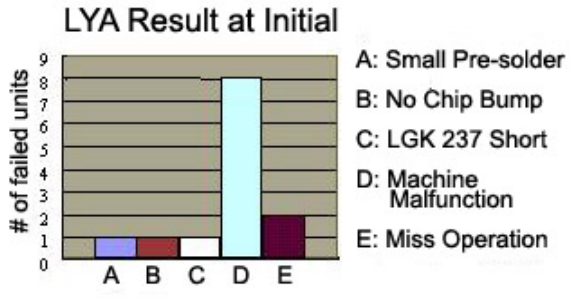

Figure 11: Failure analysis at the initial reliability test

Reliability Evaluation

Rev 1 reliability test results are summarized in Table 3. There were no electrical short failures after 100 hours of performing the Highly Accelerated Stress Test (HAST). We did observe one unit failed because of an electrical open. The open was due to poor interconnection contact that was caused by insufficient presolder volume. We believe the reason for the excellent HAST performance is the elimination of Pb in the interconnect materials.

Table 3: Rev 1 baseline reliability yield

Test	# Units Failed	Yield (%)
initial yield before reliability testing	13	95.7
T/S-B 500 cycles	5	91.7
T/S-B 1000 cycles	49	18.3
pre-condition T/C-B 500 cycles	55	0
HAST 100 hrs.	1	98.2
HAST 200 hrs.	3	94.5
steam 168 hrs.	13	82.9
steam 336 hrs.	63	17.1

The key issue of this first reliability test is the temperature cycle-B [2], T/C-B, 1000 cycle test, in which 91.7% of the samples failed due to electrical high resistance. Figure 12 shows the interface crack of the connection after T/S-B 1000 cycles.

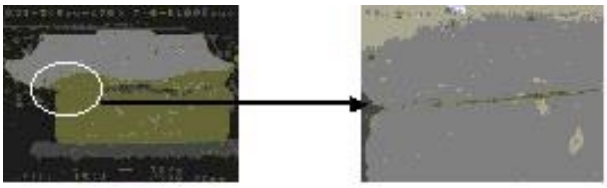

Figure 12: Interconnection crack after T/S-B 1000 cycles

Thermal Stress Issues and Improvement

In the Rev 1 baseline testing, almost all samples failed the T/C-B thermal cycle test. To improve reliability, we first modified the UF material. In the first UF modification, we compared crystal resin A with multifunctional resin B. Using a B-type resin, the UF had a higher yield due to less thermal stress between the two resins. In addition, we also compared viscosity values. Table 4 shows the electrical yield between resin types A and B.

Table 4: Reliability result for changing UF properties

UF type	A	B	Rev 1 UF
viscosity	220	300	370
T/C-B 1000 cycles	100	100	18.3
pre-condition T/C-B 500 cycles	36.8	70.0	0

Underfill A contains a crystalline resin. Underfill B and the Rev 1 underfill contain a multifunctional-type resin.

Resins A and B UF passed the T/C-B 1000 cycle test, but failed the precondition TC-B test. Figure 13 shows the relation between viscosity and percent failures.

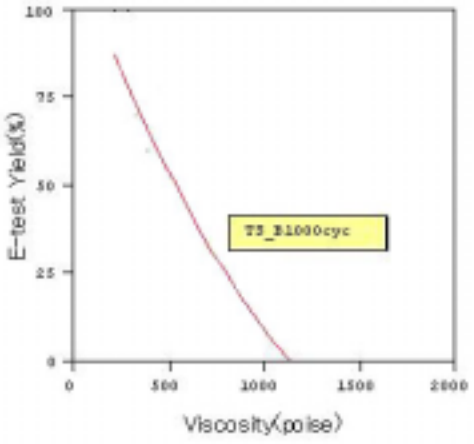

Figure 13: Yields before and after T/C-B vs. underfill viscosity

In the second UF modification, we changed filler size from 5 to 1µm. Filler residue was observed in the interface part between the die bump metal and substrate solder. Figure 14 shows the one- and five-micron filler residue at the initial condition. The 1µm filler residue in the metal interface is lower in quantity than the 5µm filler in spite of the same filler quantity being in the UF.

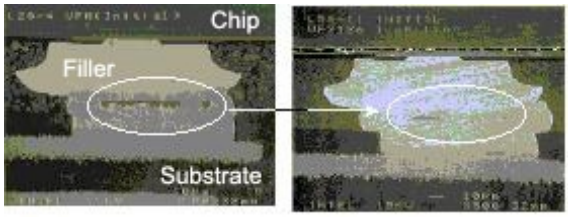

Figure 14: Filler residue at interface by filler size

We collected data on the 1µm filler and low viscosity UF for two UF materials, crystal (C) and multifunctional (D), resin. Table 5 shows that the units using 1µm filler UF showed an improved yield compared to previous baseline using 5mm filler UF.

Table 5: Data collection result of 1mm filler UF

UF type	C	D	Rev 1 UF
T/C-B 1000 cycles	100	100	18.3
pre-condition T/C-B 1000 cycles	69.4	83.3	0 (500 cycles)
interconnection side yield	100	100	

All units passed after the PCTC-B 1000 cycle test on the interconnection side. We observed a failure due to an electrical failure within the substrate side, not the interconnection side. There was no significant difference between crystal and multifunctional resin in this experiment. However, delamination between chip and UF occurred in both resins C and D more than it did in the Rev 1 baseline experiment. The 1µm filler UF properties were checked in terms of delamination. We assumed that the rubber content within the UF material changed the viscosity and caused delamination in resins C and D as shown in Table 6.

Table 6: Relation between viscosity and void and delamination percent at two viscosities

UF type	C		D		A	Rev 1
UF lot #	1	2	1	2		
viscosity 1	310	410	820	1010	1070	
viscosity 2					220	370
rubber index	75	75	100	100	100	100
void % (initial condition)	0.14	0.09	0.09	0.09	0.13	0.01
void % (after Steam 336)	13.67	8.61	6.68	6.07	0.32	0.13

Viscosity 1: 175°C, 10kgf/cm^2, Viscosity 2: 175°C, 110kgf/cm^2.

We observed a greater percentage of voids than in the Rev 1 baseline at the initial solder-join conditions. This not only caused delamination to occur because of poor adhesion after the steam reliability test, but it also caused poor UF property at the initial prereliability test.

COST DISCUSSION

Figure 15 shows the cost model estimation by Assembly Capital Equipment Development (ACED). It compares

the current POR assembly process with our three-step, no-flow process using standard cure ovens and a microwave cure oven in High Volume Manufacturing (HVM) run rates.

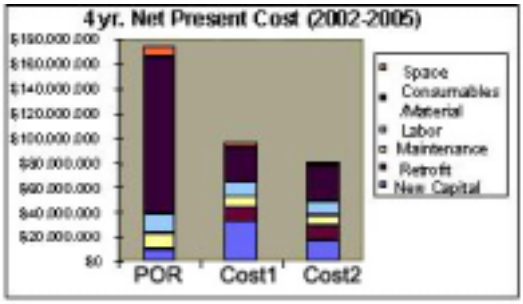

Figure 15: Assembly cost model

The columns are Cost 1: no-flow type underfill with microwave reflow and cure, and Cost 2: no flow type underfill with BTU reflow and conventional oven cure.

Both processes using no-flow type UF reduced the assembly cost when compared to the current OLGA process. We project a reduction in assembly cost over four years of $76 and $92 million when we model Cost 1 and Cost 2, respectively. The main cost savings is expected to come from material cost reduction by using no-flow UF. As a result of this process evaluation, to establish short assembly process steps, we have adjusted the assembly condition and UF material for pathfinding activities. Assembly and thermal stress tests were improved but, the delamination issue, after steam, still remains when 1μm filler UF is used. Both thermal fatigue and delamination are concerns for viscosity quantity in UF. Underfill viscosity is one important factor for thermal fatigue and delamination for this assembly using a no-flow-type UF.

When a low viscosity UF is used, the void and delamination present increased. Void at initial joint formation depends on delamination percent after the steam test. To obtain a low void and delamination percentage, we have to raise the rubber content. However, this may cause thermal fatigue to be increased by high viscosity. We should carefully set the viscosity value in new underfill materials. For future work, we need to evaluate the reliability of UF adjusted viscosity and focus more on void and delamination percentages.

CONCLUSION

A new C4 interconnection/fluxless assembly technology was proposed. The results were promising in that they demonstrated the feasibility of a one-step chip-join process that uses non-oxide forming bumps, Sn/Ag presolder, and no-flow type underfill materials. This process will reduce the number of assembly steps as well as the cost. The assembly yield was more than 90% for this pathfinding activity, and it passed an electrical test after 200 hours of HAST and 1000 cycles of PC T/C-B. We improved the assembly and reliability performance by process and material modifications as discussed.

As the C4 pad pitch shrinks and the gap between die and substrate decreases, the primary concerns are Pb electro-migration and underfilling capability for flow-type underfill materials. Using Pb for finer C4 pitch application will increase the risk of leakage by migration. There also is an effort underway to remove lead from solder in the semiconductor industry. Underfill material is dispensed to the bump gaps by capillary action. With a smaller bump gap, longer process times will be seen and may cause an increase in voids. Large die used for microprocessors present a challenge for void-free capillary underfill flow using the current POR method.

No-flow underfill material may be usable for lower C4 gap, smaller C4 pitch, and large die. An added benefit is the elimination of lead in the solder material. With a nonoxidized bump surface and substrate presolder, a good metallurgical and electrical connection without flux can be made.

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[2] Temperature cycle-B conditions taken from Mil Std. Spec 883E, method 1010.7. Temperatures are cycled between -55 °C and 125 °C.

AUTHORS' BIOGRAPHIES

Tom Dory is the package design integration engineer responsible for the next IA64 microprocessor, Mckinley, and the chipset supporting Mckinley. He earned his Ph.D. in Chemistry at the University of Oklahoma. Since joining Intel twelve years ago, he has had many responsibilities including fabrication equipment development, assembly process manufacturing, and currently new technology package design. He is also the assembly process section editor of the *Intel Assembly and*

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